SPECIFICATIONS

PCIe-5785

12-Bit, 6.4 GS/s, 2-Channel FlexRIO IF Transceiver Device

This document lists the specifications for the PCIe-5785. Specifications are subject to change without notice. For the most recent device specifications, refer to *ni.com/support*.

Note These specifications are typical at 25 °C unless otherwise noted.

Contents

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- *Typical* specifications describe the performance met by a majority of models.
- *Nominal* specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- *Measured* specifications describe the measured performance of a representative model.

Specifications are *Typical* unless otherwise noted.

Digital I/O

Connector	Molex™ Nano-Pitch I/O™
5.0 V Power	±5%, 50 mA maximum, nominal

Table 1. Digital I/O Signal Characteristics

Signal	Type	Direction
MGT Tx± <0..3>[1]	Xilinx UltraScale GTH	Output
MGT Rx± <0..3>[1]	Xilinx UltraScale GTH	Input
DIO <0..7>	Single-ended	Bidirectional
5.0 V	DC	Output
GND	Ground	—

Digital I/O Single-Ended Channels

Number of channels	8
Signal type	Single-ended
Voltage families	3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V
Input impedance	100 kΩ, nominal
Output impedance	50 Ω, nominal
Direction control	Per channel
Minimum required direction change latency	200 ns
Maximum output toggle rate	60 MHz with 100 µA load, nominal

[1] Multi-gigabit transceiver (MGT) signals are available on devices with KU040 and KU060 FPGAs only.

Table 2. Digital I/O Single-Ended DC Signal Characteristics[2]

Voltage Family	V_{IL}	V_{IH}	V_{OL} (100µA load)	V_{OH} (100µA load)	Maximum DC Drive Strength
3.3 V	0.8 V	2.0 V	0.2 V	3.0 V	24 mA
2.5 V	0.7 V	1.6 V	0.2 V	2.2 V	18 mA
1.8 V	0.62 V	1.29 V	0.2 V	1.5 V	16 mA
1.5 V	0.51 V	1.07 V	0.2 V	1.2 V	12 mA
1.2 V	0.42 V	0.87 V	0.2 V	0.9 V	6 mA

Digital I/O High-Speed Serial MGT[3]

Note MGTs are available on devices with KU040 and KU060 FPGAs only.

Data rate	500 Mbps to 16.375 Gbps, nominal
Number of Tx channels	4
Number of Rx channels	4
I/O AC coupling capacitor	100 nF

MGT TX± Channels

Minimum differential output voltage[4]	170 mV pk-pk into 100 Ω, nominal
I/O coupling	AC-coupled with 100 nF capacitor

MGT RX± Channels

Differential input voltage range	
≤ 6.6 Gb/s	150 mV pk-pk to 2000 mV pk-pk, nominal
> 6.6 Gb/s	150 mV pk-pk to 1250 mV pk-pk, nominal
Differential input resistance	100 Ω, nominal
I/O coupling	DC-coupled, requires external capacitor ⚠

[2] Voltage levels are guaranteed by design through the digital buffer specifications.
[3] For detailed FPGA and High-Speed Serial Link specifications, refer to Xilinx documentation.
[4] 800 mV pk-pk when transmitter output swing is set to the maximum setting.

Reconfigurable FPGA

PCIe-5785 modules are available with multiple FPGA options. The following table lists the FPGA specifications for the PCIe-5785 FPGA options.

Table 3. Reconfigurable FPGA Options

	KU035	KU040	KU060
LUTs	203,128	242,200	331,680
DSP48 slices (25 × 18 multiplier)	1,700	1,920	2,760
Embedded Block RAM	19.0 Mb	21.1 Mb	38.0 Mb
Data Clock Domain	200 MHz, 16 samples per cycle per channel (dual channel mode), 32 samples per cycle (single channel mode)		
Timebase reference sources	Onboard 100 MHz oscillator		
Data transfers	DMA, interrupts, programmed I/O	DMA, interrupts, programmed I/O, multi-gigabit transceivers	
Number of DMA channels	60		

Note The Reconfigurable FPGA Options table depicts the total number of FPGA resources available on the part. The number of resources available to the user is slightly lower, as some FPGA resources are consumed by board-interfacing IP for PCI Express, device configuration, and various board I/O. For more information, contact NI support.

Onboard DRAM

Memory size	4 GB (2 banks of 2 GB)
DRAM clock rate	1064 MHz
Physical bus width	32 bit
LabVIEW FPGA DRAM clock rate	267 MHz
LabVIEW FPGA DRAM bus width	256 bit per bank
Maximum theoretical data rate	17 GB/s (8.5 GB/s per bank)

Analog Input

General Characteristics

Number of channels	2, single-ended, simultaneously sampled
Connector type	SMA
Input impedance	50 Ω
Input coupling	AC
Sample Clock	
Internal Sample Clock	3.2 GHz
External Sample Clock	2.8 GHz to 3.2 GHz
Sample Rate	
Dual channel mode	3.2 GS/s per channel
Single channel mode	6.4 GS/s
Analog-to-digital converter (ADC)	ADC12DJ3200, 12-bit resolution
Input latency[5]	239 ns

Typical Specifications

Full-scale input range	1.25 V pk-pk (5.92 dBm) at 10 MHz
AC gain accuracy	±0.11 dB at 10 MHz
DC offset	±2.19 mV
Bandwidth (-3 dB)[6]	500 kHz to 6 GHz

Table 4. Single-Tone Spectral Performance, Dual Channel Mode

	Input Frequency				
	99.9 MHz	**399 MHz**	**999 MHz**	**1.999 GHz**	**2.499 GHz**
SNR[7] (dBFS)	56.0	55.6	54.7	52.9	51.6
SINAD[7] (dBFS)	55.5	55.0	54.0	51.8	50.8

[5] SMA input to LabVIEW diagram
[6] Normalized to 10 MHz.
[7] Measured with a -1 dBFS signal and corrected to full-scale. 3.2 kHz resolution bandwidth.

Table 4. Single-Tone Spectral Performance, Dual Channel Mode (Continued)

	Input Frequency				
	99.9 MHz	**399 MHz**	**999 MHz**	**1.999 GHz**	**2.499 GHz**
SFDR (dBc)	-64.9	-63.4	-62.7	-59.9	-58.6
ENOB[8] (bits)	8.9	8.8	8.7	8.3	8.1

Table 5. Single-Tone Spectral Performance, Single Channel Mode[9]

	Input Frequency				
	99.9 MHz	**399 MHz**	**999 MHz**	**1.999 GHz**	**2.499 GHz**
SNR[7] (dBFS)	54.6	54.2	52.4	49.7	48.9
SINAD[7] (dBFS)	54.4	53.9	52.1	49.4	48.6
SFDR (dBc)	-61.7	-60.4	-56.1	-51.7	-51.1
ENOB[8] (bits)	8.7	8.7	8.4	7.9	7.8

Table 6. Noise Spectral Density[10]

Mode	$\frac{nV}{\sqrt{Hz}}$	$\frac{dBm}{Hz}$	$\frac{dBFS}{Hz}$
Dual channel	14.4	-143.8	-149.2
Single channel	9.8	-147.2	-152.6

Note Noise spectral density is verified using a 50 Ω terminator connected to the input.

[8] Calculated from SINAD and corrected to full scale.
[9] Measured using channel AI0. Spectral performance may be degraded using channel AI1.
[10] Excludes fixed interleaving spur (Fs/2 spur).

Figure 1. Single Tone Spectrum (Dual Channel Mode, 99.9 MHz, -1 dBFS, 3.2 kHz RBW), Measured

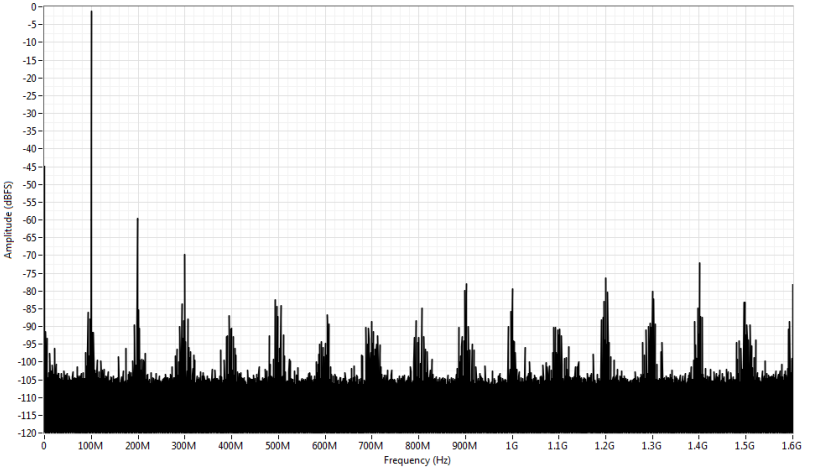


Figure 2. Single Tone Spectrum (Dual Channel Mode, 1.999 GHz, -1 dBFS, 3.2 kHz RBW), Measured

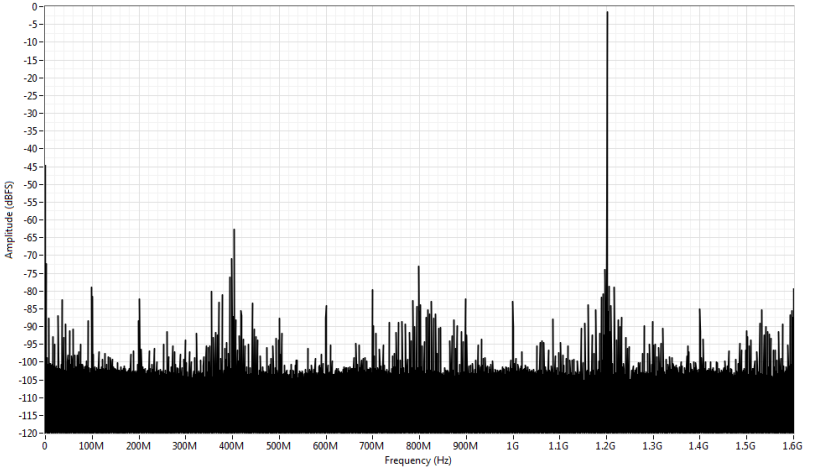


Figure 3. Single Tone Spectrum (Single Channel Mode, 99.9 MHz, -1 dBFS, 3.2 kHz RBW), Measured

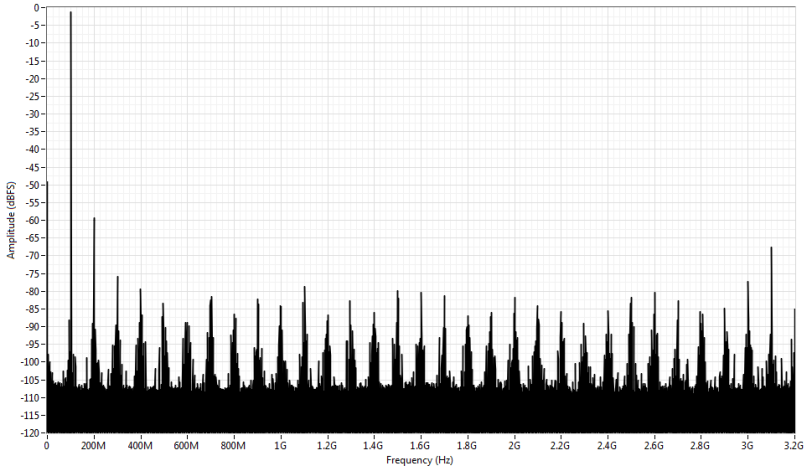
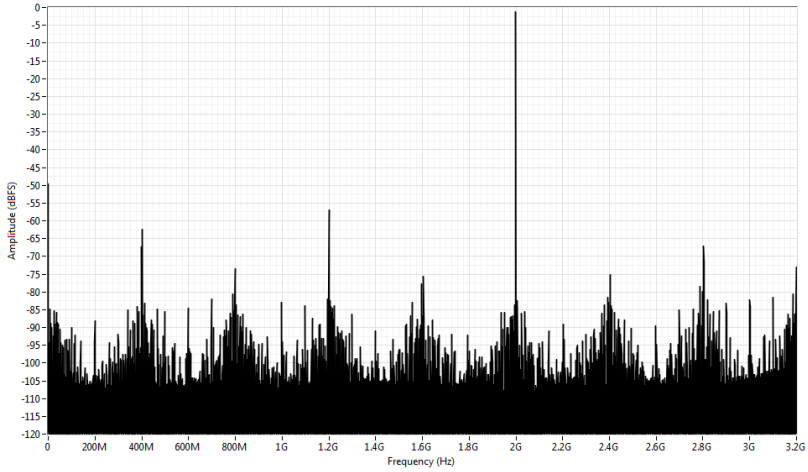


Figure 4. Single Tone Spectrum (Single Channel Mode, 1.999 GHz, -1 dBFS, 3.2 kHz RBW), Measured



Channel-to-channel crosstalk, measured	
99.9 MHz	-92.5 dB
399 MHz	-85.5 dB
999 MHz	-76.5 dB

1.999 GHz	-68.8 dB
2.499 GHz	-67.4 dB

Figure 5. Analog Input Frequency Response, Measured

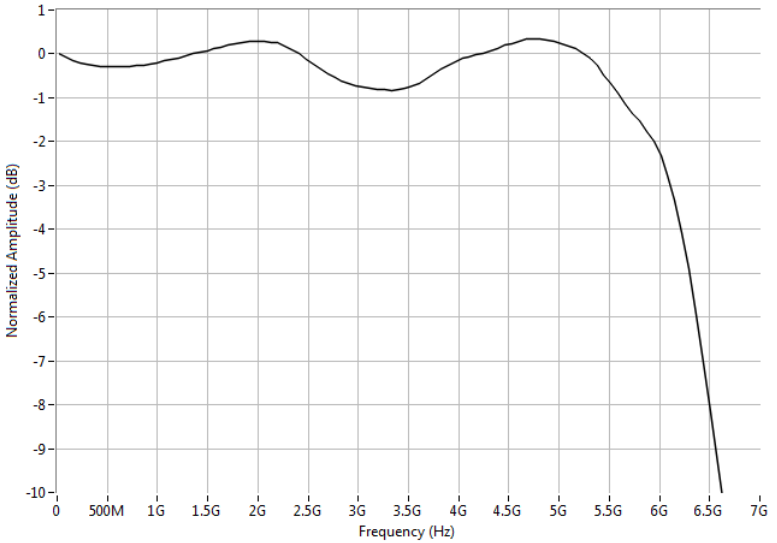
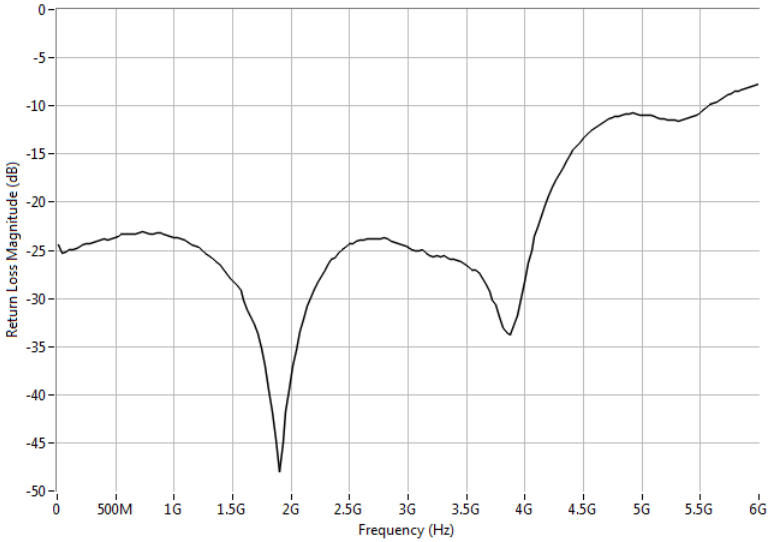


Figure 6. Input Return Loss, Measured



Analog Output

General Characteristics

Number of channels	2, single-ended, simultaneously updated
Connector type	SMA
Output impedance	50 Ω
Output coupling	AC
Update rate	
Internal Sample Clock, 2x interpolation	6.4 GS/s
External Sample Clock, 2x interpolation	6.4 GS/s[11]

[11] To achieve this update rate when using an external sample clock, inject a 3.2 GS/s clock into the REF/CLK IN port and enable 2x interpolation.

Data rate (per channel)	
Dual channel mode	3.2 GS/s, real
Single channel mode	3.2 GS/s, complex
Digital-to-analog converter (DAC)	DAC38RF82, 12-bit resolution
Output latency[12]	
DUC disabled	211 ns
DUC enabled	221 ns

Typical Specifications

Note Due to a silicon flaw in the TI DAC38RF82 chip, there is a 0.5% chance of seeing a 50 mV glitch at the output of either channel after a bitfile re-download, invoking the Reset method explicitly or by closing the FPGA reference, or committing a new configuration.

Full-scale output power[13]	
Dual Channel Mode	2.85 dBm (878 mVpp)
Single Channel Mode	-3.33 dBm (431 mVpp)
Bandwidth (-3 dB)[14]	
Dual Channel Mode	3 MHz to 1.53 GHz
Single Channel Mode (no anti-image filter)	60 MHz to 2.85 GHz
Single Channel Mode (with anti-image filter)	60 MHz to 2.35 GHz

Table 7. Single Tone Spectral Performance, Dual Channel Mode[15]

	Generation Frequency	
	501 MHz	**1.01 GHz**
2nd HD (dBc)	-67.8	-61.7
3rd HD (dBc)	-63.0	-62.0
SFDR (dBc)	-63.0	-61.7

[12] LabVIEW diagram to SMA output

[13] Into a 50 Ω load.

[14] Normalized to 10 MHz in dual channel mode and 200 MHz in single channel mode. 2x interpolation and inverse sinc filter enabled.

[15] DC, 3.2 GHz, output corrected to 0 dBFS by inverse sinc filter, 2x interpolation, no anti-image filter.

Table 8. Single Tone Spectral Performance, Single Channel Mode[15]

	Generation Frequency
	1.01 GHz
2nd HD (dBc)	-62.4
3rd HD (dBc)	-67.3
SFDR (dBc)	-62.4

Table 9. IMD3 Performance, Dual Channel Mode, Measured[16]

	Generation Frequency	
	501 MHz and 511 MHz	1.005 GHz and 1.015 GHz
IMD3 (dBc)	-73.9	-67.6

Table 10. Noise Spectral Density[17]

	501 MHz Generation Frequency		
Mode	$\frac{nV}{\sqrt{Hz}}$	$\frac{dBm}{Hz}$	$\frac{dBFS}{Hz}$
Dual Channel	1.18	-165.5	-168.4
Single Channel	0.941	-167.5	-164.2

16 2x interpolation, inverse sinc filter enabled, each tone corrected to -6 dBFS by inverse sinc filter.

17 Measured > 50 MHz offset from fundamental. 2x interpolation and inverse sinc filter enabled. Noise spectral density value depends on output tone frequency. See DAC38RF82 datasheet for noise spectral density results at other tone frequencies.

Figure 7. Single Tone Spectrum (Dual Channel Mode, 501 MHz 0 dBFS), Measured[18]

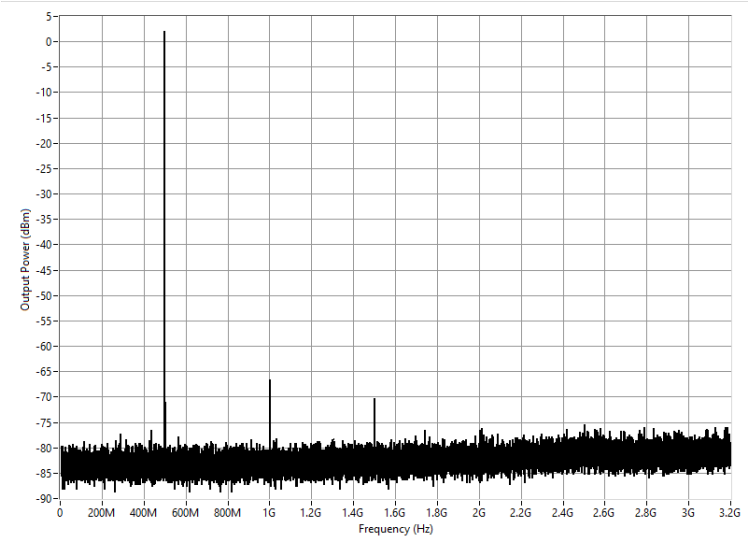
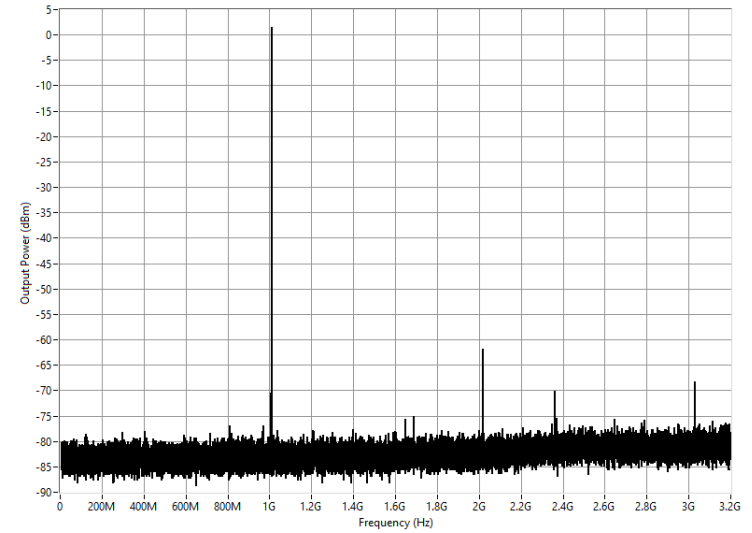
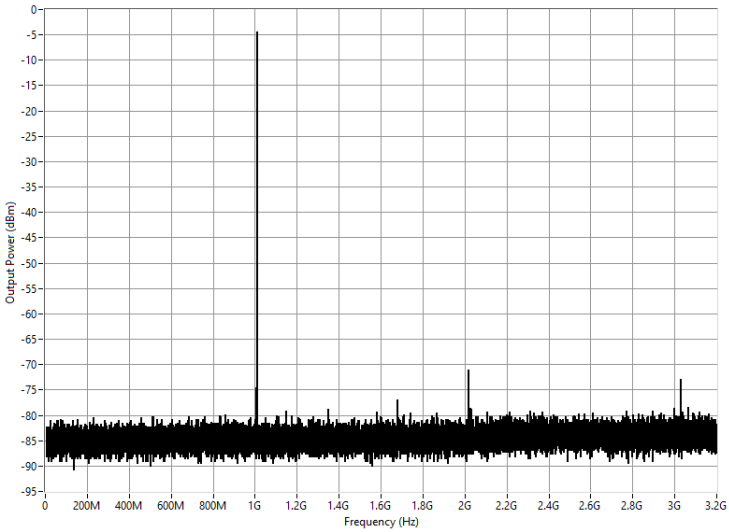


Figure 8. Single Tone Spectrum (Dual Channel Mode, 1.01 GHz 0 dBFS), Measured[18]



[18] 2x interpolation. Output corrected to 0 dBFS by inverse sinc filter. 10 kHz resolution bandwidth.

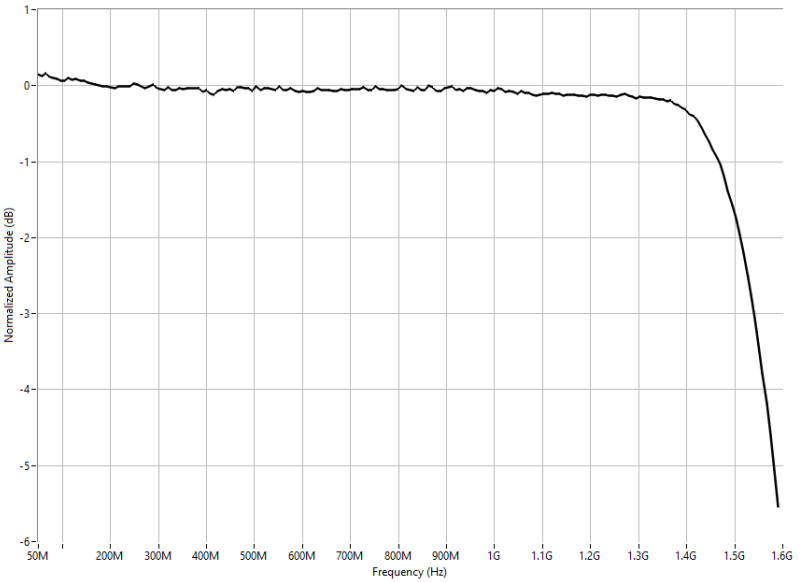
Figure 9. Single Tone Spectrum (Single Channel Mode, 1.01 GHz 0 dBFS), Measured[18]



Channel-to-channel crosstalk, measured[19]	
100 MHz	-82 dBc
500 MHz	-91 dBc
1.0 GHz	-90 dBc
1.5 GHz	-88 dBc
2.0 GHz	-82 dBc
2.5 GHz	-82 dBc

[19] Aggressor channel generating a full-scale output into a 50 ohm terminator

Figure 10. Analog Output Dual Channel Mode Frequency Response, Measured [20]



[20] -6 dBFS, 2x Interpolation, inverse sinc filter enabled, no anti-image filter, normalized to 200 MHz.

Figure 11. Analog Output Single Channel Mode Frequency Response, No Anti-Image Filter, Measured[20]

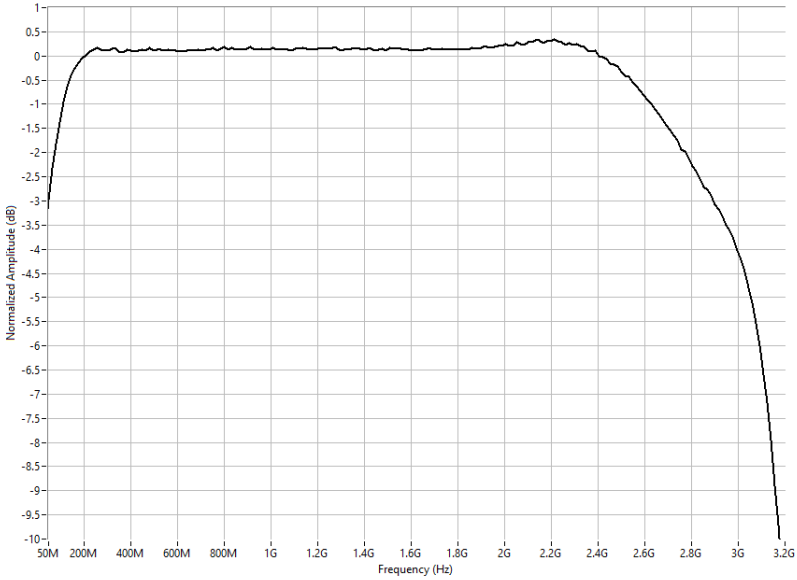
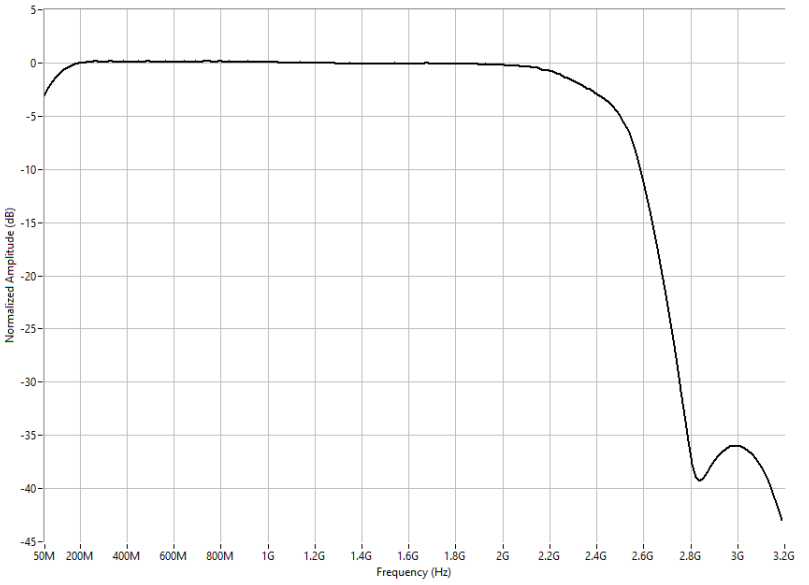
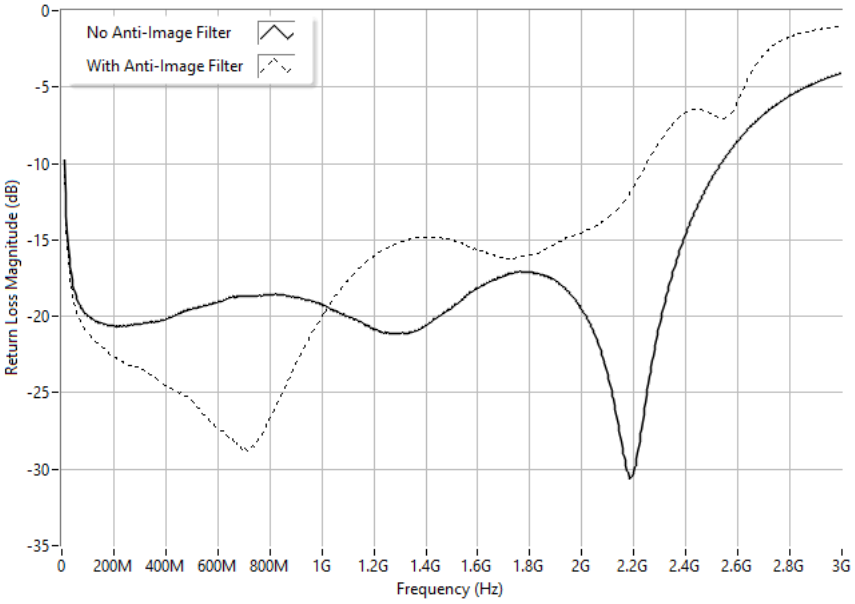


Figure 12. Analog Output Single Channel Mode Frequency Response With Anti-Image Filter, Measured[21]



[21] -6 dBFS, 2x Interpolation, inverse sinc filter enabled, normalized to 200 MHz.

Figure 13. Analog Output Return Loss, Measured



REF/CLK IN

General Characteristics

Connector type	SMA
Input impedance	50 Ω
Input coupling	AC
Input voltage range	0.35 V pk-pk to 3.5 V pk-pk, nominal
Absolute maximum voltage	±12 V DC, 4 V pk-pk AC
Duty cycle	45% to 55%

Sample Clock jitter	
Analog input	86.8 fs_{rms}, measured[22]
Analog output	198.8 fs_{rms}, measured[23]

Table 11. Clock Configuration Options

Clock Configuration	External Clock Frequency	Description
Internal Baseboard Reference Clock[24]	10 MHz	The internal Sample Clock locks to the 10 MHz Reference Clock provided from the FPGA baseboard.
External Reference Clock (REF/CLK IN)	10 MHz[25]	The internal Sample Clock locks to an external Reference Clock, which is provided through the REF/CLK IN front panel connector.
External Sample Clock (REF/CLK IN)	2.8 GHz to 3.2 GHz	An external Sample Clock can be provided through the REF/CLK IN front panel connector.

22 Integrated from 3.2 kHz to 20 MHz. Includes the effects of the converter aperture uncertainty and the clock circuitry jitter. Excludes trigger jitter.

23 Integrated from 1 kHz to 30 MHz. Includes the effects of the converter aperture uncertainty, converter PLL circuitry, and the clock circuitry jitter. Excludes trigger jitter.

24 Default clock configuration.

25 The external Reference Clock must be accurate to ±25 ppm.

Figure 14. Analog Input Phase Noise with 800 MHz Input Tone, Measured

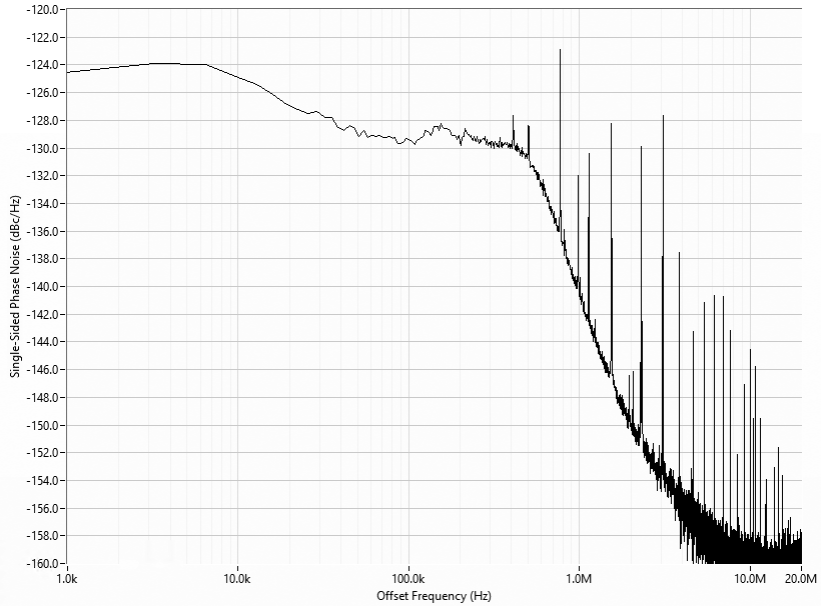
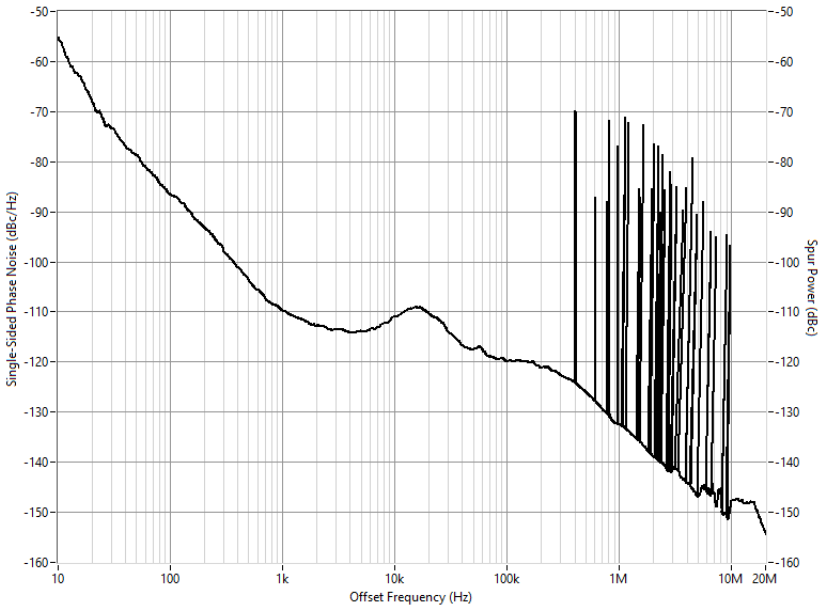


Figure 15. Analog Output Phase Noise with 1 GHz Output Tone, Measured



Bus Interface

Card edge form factor	PCI Express Gen-3 x8
Slot compatibility	x8 and x16 PCI Express slots

Maximum Power Requirements

Note Power requirements are dependent on the contents of the LabVIEW FPGA VI used in your application.

+3.3 V	4.5 A
+12 V	5 A
Maximum total power	75 W

Physical

Dimensions (including I/O bracket, not including connectors)	12.6 cm × 26.3 cm × 4 cm (5.0 in. × 10.4 in. × 1.6 in.)
Weight	990 g (35 oz)
PCI Express mechanical form factor	Standard height, three-quarter length, double slot
Integrated air mover (fan)	Yes
Maximum rear panel exhaust airflow	84 m^3/h (50 CFM) (without any chassis impedance)

Environmental

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution degree	2

Indoor use only.

Operating Environment

Operating temperature, local[26]	0 °C to 45 °C
Operating humidity	10% to 90% RH, noncondensing

Storage Environment

Ambient temperature range	-20 °C to 70 °C
Relative humidity range	5% to 95% RH, noncondensing

[26] For PCI Express adapter cards with integrated air movers, NI defines the local operational ambient environment to be at the fan inlet. For cards without integrated air movers, NI defines the local operational ambient environment to be 25 mm (1 in.) upstream of the leading edge of the card.

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